IPSmart

12-Bit 50 MSPS ADC in IBM 180 SOI

IPS_I180_ADC12_50M

FEATURES

- **Single Supply 1.5V**
- **50 MSPS Conversion Rate**
- **Current Consumption**
  60 mW @ 50 MSPS
- **Dynamic Performance @ 50MSPS**
  66 dBFS SNR
  -69 dBc THD
  70 dBc SFDR
  ENOB of 10.2
- **Programmable current setting**
- **Programmable full scale**
- **Ultra Small Core Area: 800um X 350 um= 0.28 mm^2**
- **IBM 180nm SOI**

APPLICATIONS

- **WiFi, HDTV, Video Application**
- **Communication RX Channel**
- **Digital Imaging**

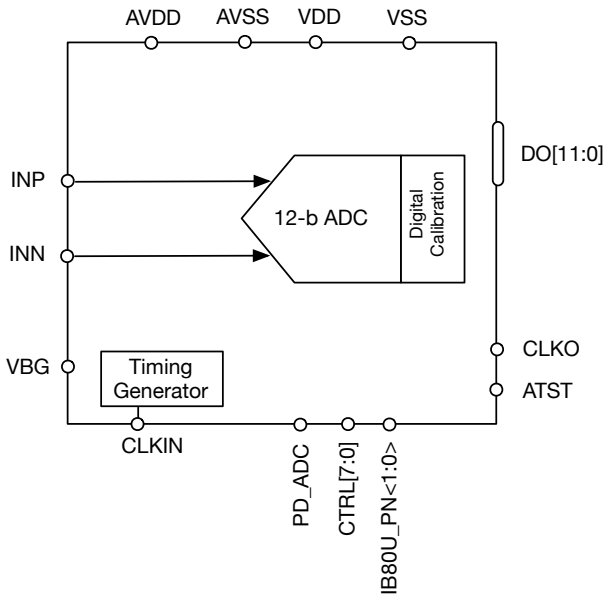

Figure 1. BLOCK DIAGRAM

GENERAL DESCRIPTION

IPS_I180_ADC12_50M is compact and low power 12-bit analog-to-digital converter silicon IP. This ADC uses 1.5b/stage pipelined architecture optimized for low power and small area. This ADC uses fully differential pipelined architecture optimized for low power and small area. The ADC is designed for high dynamic performance. This ADC consumes 60 mW at 50 MSPS operation and occupies silicon area of 0.28 mm^2. The ADC has high immunity to substrate noise and is ideal for integration into SoC.

PIN DESCRIPTION

Pin Function Descriptions

Index	Pin Name	I/O	Description
1	AVDD	AP	Analog power supply 1.5V
2	VDD	DP	Digital power supply 1.5V
3	AVSS	AG	Analog ground
4	VSS	DG	Digital ground
5	INP, INN	AI	Analog differential inputs
6	CLKIN	DI	Input clock
7	PD_ADC	DI	ADC power down mode, all blocks are disabled
8	CLKO	DO	Output clock, can be used to sample DATA[11:0]
9	DO[11:0]	DO	12-bit output data of ADC
10	ATST	AO	Analog test point
11	VBG	AI	Bandgap voltage input
12	IB80U_PN<1:0>	AI	80UA current reference from Bandgap (PMOS → NMOS)
13	CTRL[7:0]	DI	ADC programmability and control bits

P: Power, **G:** Ground, **A**: Analog, **D**: Digital, **I**: input, **O**: Output

PHYSICAL DESCRIPTION

IP macro layout.