IPSmart

Triple 10-bit 330 MSPS Video DAC IP in 90 nm

IPS_T90_DAC10X3_330M

FEATURES

- 10-bit Resolution
- Up to 330 MSPS Conversion Rate
- Dual 3.3 V and 1.2V Power Supply
- Current Consumption
  41 mA/Channel @ I_{FS} = 34mA
- DNL < ± 1 LSB, INL < ± 2 LSB
- Single-Ended or Differential Output
- Full Scale output current: 17mA to 34mA
- 1.3V output swing – Single ended
- 6-bit Programmable Full-scale Current
- Cable connection detect per channel
- Small Core Area: 0.33 mm^2
- TSMC 90 nm 6 Metal (3.3V IO)

APPLICATIONS

- Composite Video (CVBS)
- HDTV
- RGB Video

GENERAL DESCRIPTION

IPS_T90_DAC10X3_330M is a 10-bit Triple DAC designed in TSMC 90 nm logic process. It consists of a current steering DAC. The DAC uses a fully differential architecture. The input data of the DAC is in 1.2 V, in unsigned format.

BLOCK DIAGRAM

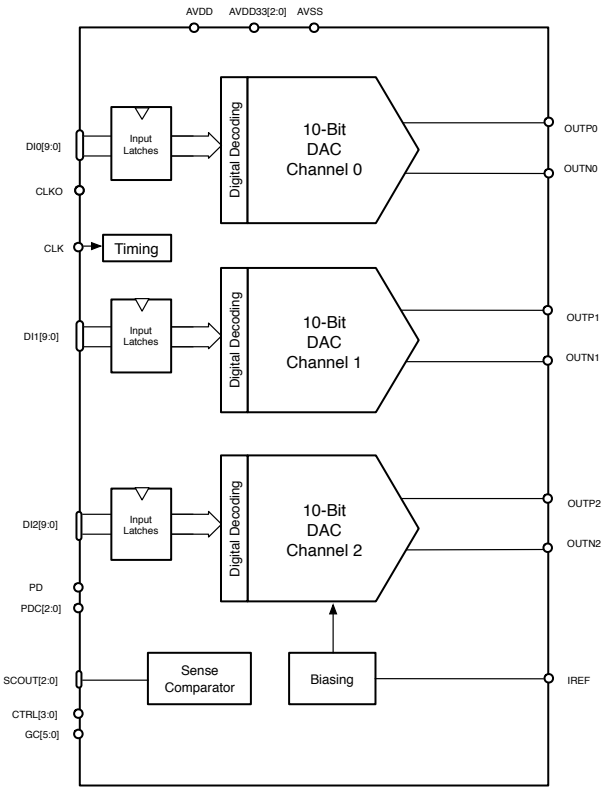


Fig. 1. Functional block diagram.

A 3.3 V supply is used for the analog portion of the IP. This high performance DAC is designed for CVBS standard or RBG Video signal bandwidth. The IP consumes only 41 mA per channel at 330 MSPS operation and utilizes a silicon area of only 0.33 mm^2. The IP does not require any external decoupling and is ideal for integration in mixed-signal systems. The IP is easily reconfigurable from single channel to 4-channel Video DAC.

PIN DESCRIPTION

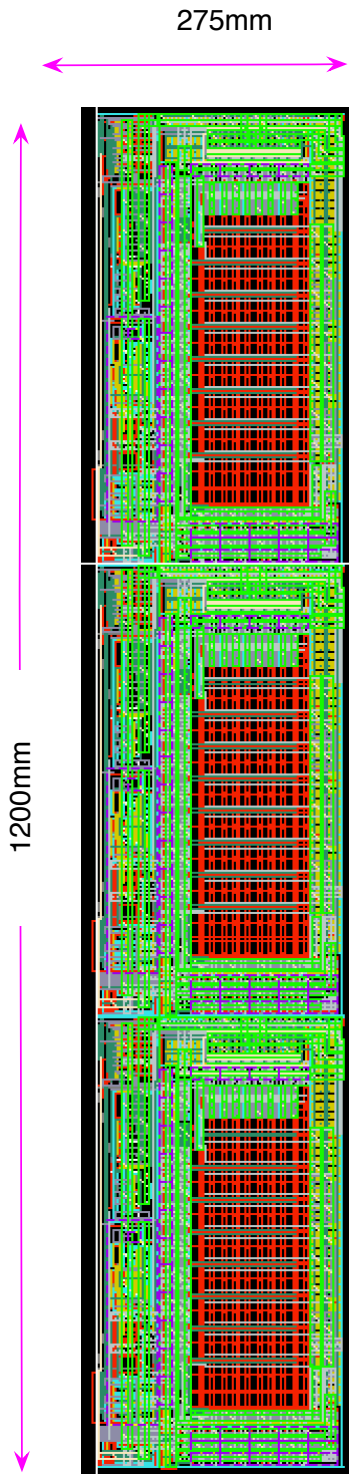
Pin Function Descriptions (total 22 pins)

Pin Name	I/O	Description
OUTP2, OUTP1, OUTP0, OUTN2, OUTN1, OUTN0	AO	Differential analog outputs for DAC
AVDD33_2, AVDD33_1, AVDD33_0	AP	3.3 V DAC power supply
AVDD	AP	1.2V DAC power supply
AVSS	AG	DAC analog ground
IREF	AI	Input reference current (500 μA sink) or external resistor 1.24 K to ground
PD	DI	Master Power-down control (logic 1 → power-down)
GC[5:0]	DI	DAC output current gain control bits, the minimum is 17mA for all zeros, the maximum is 34mA for all ones
PDC[2:0]	DI	Power-down control for each channel
CTRL[3:0]	DI	DAC Control Bits
DI0[9:0], DI1[9:0], DI2[9:0].	DI	10-bit input data of DAC for each channel
CLKO	DO	Output clock
SCOUT[2:0]	DO	Cable connection sense comparator output (if voltage is greater than 350mV)
CLK	DI	Input clock

P: Power, **G:** Ground, **A**: Analog, **D**: Digital, **I**: input, **O**: Output

Note: All the digital inputs and outputs are in core voltage 1.2V domain.

PHYSICAL DESCRIPTION



PREVIOUS SILICON RESULT