IPSmart

12-Bit 125 MSPS Duel ADC in SMIC40L

IPS_S40L_ADC12X2_125M

FEATURES

- **Single Supply 1.15V**
- **125 MSPS Conversion Rate**
- **Current Consumption**
  45 mW @ 125 MSPS
- **Dynamic Performance @ 125MSPS**
  65 dBFS SNR
  -68 dBc THD
  70 dBc SFDR
  ENOB of 10.2
- **Programmable current setting**
- **Programmable full scale**
- **Ultra Small Core Area: 600um X 550 um= 0.33 mm^2**
- **SMIC 40LP 1P6M**

APPLICATIONS

- **WiFi, HDTV, Video Application**
- **Communication RX Channel**
- **Digital Imaging**

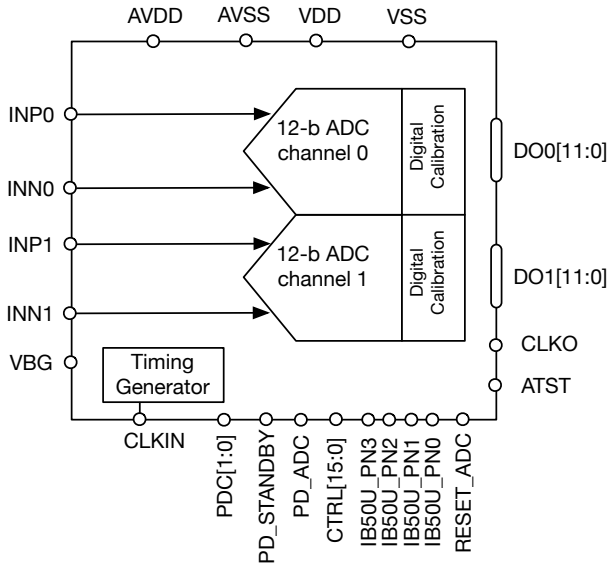

Figure 1. BLOCK DIAGRAM

GENERAL DESCRIPTION

S40L_ADC12X2_125M is compact and low power 12-bit analog-to-digital converter silicon IP. This ADC uses 1.5b/stage pipelined architecture optimized for low power and small area. This ADC uses fully differential pipelined architecture optimized for low power and small area. The ADC is designed for high dynamic performance. This ADC consumes 45 mW at 125 MSPS operation and occupies silicon area of 0.33 mm^2. The ADC has high immunity to substrate noise and is ideal for integration into SoC.

DC SPECIFICATIONS

T_j = 25˚C, AVDD = 1.15 V, f_{IN} = 10 MHz, f_S= 125 MHz, A_{IN} = -1 dBFS, unless otherwise noted.

Table 1. DC Performance

Parameter	Test Conditions	Test	Min	Typ	Max	Unit
Resolution		B		12		bits
Monotonicity		B		Guaranteed		
Differential Nonlinearity (DNL)		B		±0.6	±1	LSB
Integral Nonlinearity (INL)		B		±2	±3	LSB
Input Common-Mode Voltage		B	0.45	0.55		V
Input Differential Voltage Range		B		0.9		Vpp
Input Capacitance	single-ended	B		2		pF
Absolute Gain Accuracy		B		±0.5		% FS
Phase mismatch		B		0.5		Degree
Offset Error		B		±4		LSB
Operating Junction Temperature (Tj)		A(1)	-40		125	˚C
Analog Supply Voltage AVDD		B	1.09	1.15	1.21	V
AVDD Supply Current		B	36	39	46	mA
Digital Supply Voltage VDD		B	0.99	1.1	1.21	V
Power Dissipation		B	39	45	56	mW
Power Down Current		B	12	15	40	uA

(1) Measurement temperature 0~85C

AC SPECIFICATIONS

T_j = 25˚C, AVDD = 1.15 V, f_{IN} = 10 MHz, f_S= 125 MHz, A_{IN} = -1 dBFS, unless otherwise noted.

Table 2. AC Performance

Parameter	Test conditions	Test	Min	Typ	Max	Unit
Maximum Conversion Rate		B	125			MHz
Analog Input Bandwidth		B		200		MHz
Signal-to-Noise Ratio (SNR)		B	62	65		dBFS
Spurious Free Dynamic Range (SFDR)		B	68	70		dBc
Total Harmonic Distortion (THD)		B	-64	-68		dBc
Signal-toNoise Distortion (SNDR)		B	60	63		dBFS
ENOB		B	9.6	10.2		Bits
Channel Isolation		B	70			dBc
Wake-up Time from Standby mode		B		100		ns
Start-up Time from Power Down mode		B		1		us

Test Categories

A. Preliminary target specification.

B. Simulation of the design over process, voltage, and temperature (PVT)[(1)].

C. Measurements on a set of samples at typical process over voltage and temperature.

D. Measurements on a set of samples at process corners over voltage and temperature.

PIN DESCRIPTION

Table 6. Pin Function Descriptions (total 23 pins)

Index	Pin Name	I/O	Description
1	AVDD	AP	Analog power supply 1.15V from LDO
2	VDD	DP	Digital power supply 1.1V
3	AVSS	AG	Analog ground
4	VSS	DG	Digital ground
5	I_INP/I_INN	AI	I channel differential inputs
6	Q_INP/Q_INN	AI	Q channel differential inputs
7	CLKIN	DI	Input clock
8	PDC[1:0]	DI	ADC channel enable control input (logic 1 → power down)
9	PD_STANDBY	DI	ADC standby mode, clock and OPAMP are disabled
10	PD_ADC	DI	ADC power down mode, all blocks are disabled
11	CLKO	DO	Output clock, can be used to sample DATA[11:0]
12	DO0[11:0], DO1[11:0]	DO	IQ 12-bit output data of ADC
13	ATST	AO	Analog test point
14	VBG	AI	Bandgap voltage input
15	IB50U_PN3, IB50U_PN2, IB50U_PN1, IB50U_PN0	AI	50UA current reference from Bandgap (PMOS → NMOS)
16	RESET_ADC	DI	Clock divider RESET signal
17	CTRL[15:0]	DI	ADC programmability and control bits

P: Power, **G:** Ground, **A**: Analog, **D**: Digital, **I**: input, **O**: Output

PHYSICAL DESCRIPTION

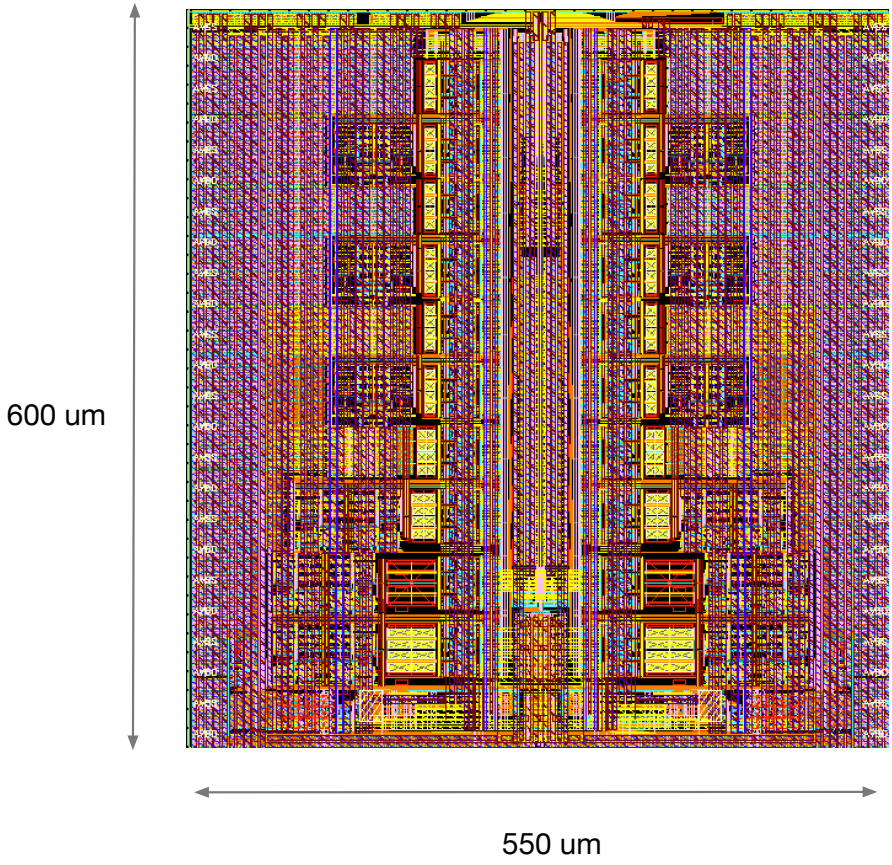

Fig. 6. IP macro layout.