IPSmart

14-Bit 3 MSPS ADC in GSMC110nm

IPS_GS110_ADC14_3M

FEATURES

- **Wide Supply Range 1.7 V to 5.6V**
- **14bit, up to 3 MSPS Conversion Rate**
- **Low Power Consumption**
  150 uA @ 3 MSPS
- **Dynamic Performance @ 3MSPS**
  72 dBFS SNR
  -72 dBc THD
  74 dBc SFDR
  ENOB of 11.2
- **20 single-ended inputs or 10 differential inputs**
- **Internal reference option**
- **Ultra Small Core Area: 0.32 mm^2**
- **GSMC 110nm 1P5M**

APPLICATIONS

- **General purpose data acquisition**
- **Battery monitory system**
- **Temperature monitory system**

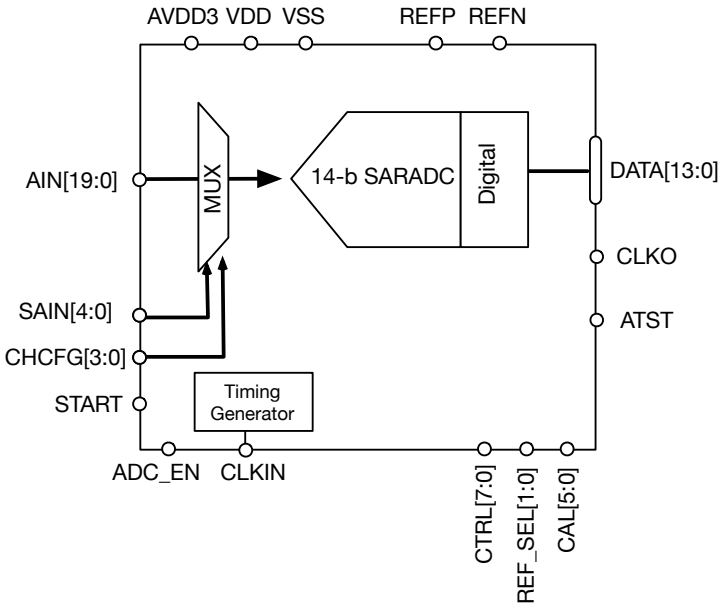

Figure 1. BLOCK DIAGRAM

GENERAL DESCRIPTION

IPS_GS110_ADC14_3M is compact and low power 14-bit analog-to-digital converter silicon IP. It has 20 single-end input channel selection multiplexer or 10 differential input channels selection. This ADC uses fully differential SAR architecture optimized for low power and small area. The ADC is designed for high dynamic performance for input frequencies up to Nyquist rate. This ADC consumes 150 uA at 3 MSPS operation and occupies silicon area of 0.32 mm^2. The ADC has high immunity to substrate noise and is ideal for SoC integration.

PIN DESCRIPTION

Pin Function Descriptions

Index	Pin Name	I/O	Description
1	AVDD3	AP	Analog power supply 1.7V to 5.6V, default is 3.3V
2	VDD	DP	Digital power supply 1.5V
3	VSS	DG	ADC ground
4	REFP	AI	Positive reference voltage connecting to AVDD3
5	REFN	AI	Negative reference voltage connecting to VSS
6	CLKIN	DI	Input clock, note that input clock frequency is the sampling rate
7	AIN[19:0]	AI	Analog inputs channels
8	CHCFG[3:0]	DI	Channel configuration control bits
9	SAIN[4:0]	DI	Input channel select bits
10	REF_SEL[1:0]	DI	Internal reference voltage selection (2V, 3V or 4V)
11	START	DI	Start of conversion
12	ADC_EN	DI	ADC enable control input (logic 1 → power up, logic 0 → power down)
13	CLKO	DO	Output clock, can be used to sample DATA[13:0]
14	DATA[13:0]	DO	14-bit output data of ADC
15	CTRL[7:0]	DI	Internal reference and speed control bits
16	CAL[5:0]	DI	Cap mismatch calibration control bits
17	ATST	AO	Analog test output

P: Power, **G:** Ground, **A**: Analog, **D**: Digital, **I**: input, **O**: Output

PHYSICAL DESCRIPTION

IP Macro Layout: 620 um X 520 um