IPSmart

10-Bit 165 MSPS ADC in TSMC110nm

IPS_T110_ADC10_165M

FEATURES

- **Single Supply 1.2V**

- **165 MSPS Conversion Rate**

- **Current Consumption**
  - **36 mA @ 165 MSPS**

- **Dynamic Performance @ 165MSPS**
  - **58 dBFS SNR**
  - **-60 dBc THD**
  - **62 dBc SFDR**
  - **ENOB of 9.0**

- **Programmable current setting**

- **Programmable ADC full scale**

- **Internal Bandgap reference**

- **Ultra Small Core Area: 0.21 mm^2**

- **TSMC 110/130nm 1P5M**

APPLICATIONS

- **Communication RX Channel**

- **RGB, HDTV, Video Application**

- **Digital Imaging**

Figure 1. BLOCK DIAGRAM

GENERAL DESCRIPTION

IPS_T110_ADC10_165M is compact and low power 10-bit analog-to-digital converter silicon IP. This ADC uses 1.5b/stage pipelined arch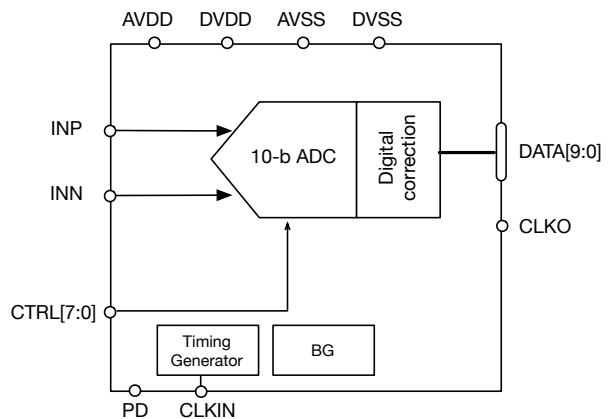itecture and it is optimized for low power and small area. The ADC is designed for high dynamic performance for input frequencies up to Nyquist rate. This ADC consumes 36 mA at 165 MSPS operation and occupies silicon area of 0.21 mm^2. The ADC has high immunity to substrate noise and is ideal for SoC integration.

PIN DESCRIPTION

Index	Pin Name	I/O	Description
1	AVDD	AP	Analog power supply 1.2V
2	DVDD	DP	Digital power supply 1.2V
3	AVSS	AG	Analog ground
4	DVSS	DG	Digital ground
5	INP/INN	AI	Analog differential inputs
6	CLKIN	DI	Input clock
7	PD	DI	ADC enable control input (logic 0 → power up, logic 1 → power down)
8	CLKO	DO	Output clock, can be used to sample DATA[9:0]
9	DATA[9:0]	DO	10-bit output data of ADC
10	CTRL[7:0]	DI	Programmable current setting and ADC full scale control bits

P: Power, **G:** Ground, **A**: Analog, **D**: Digital, **I**: input, **O**: Output

PHYSICAL DESCRIPTION

700 um

300 um

Rev. 1.0