IPSmart

12-Bit 320MSPS IQ DAC in SMIC 40nm L

IPS_S40_DAC12X2_320M

FEATURES

- **Dual 12-bit DAC, up to 320 MSPS**
- **Dual 3.3 V / 1.15 V Supply**
- **Low Power Consumption**
  55mW @ 320 MSPS
- **Superior Dynamic Range**
  71dBc SFDR @ f_{out} = 40 MHz
- **IFS = 6mA with programmability**
- **Output voltage: 1Vppd**
- **Programmable termination resistor**
- **Ultra Small Core Area: 460um X 460um= 0.21 mm^2**
- **SMIC 40LP 1P6M**

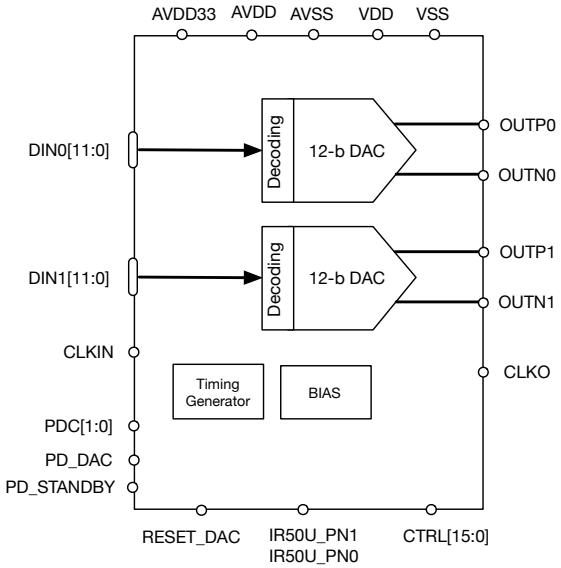

Figure 1. BLOCK DIAGRAM

APPLICATIONS

- **WiFi / LTE / WiMax**
- **Wireless MIMO**
- **Digital Video**
- **Communication Transmit**

GENERAL DESCRIPTION

S40L_DAC12X2_320M is compact and low power 12-bit digital-to-analog converter silicon IP in SMIC 40nm LP process. It features two channel current steering DAC.

This IQ DAC IP is optimized for low power and small area. At 320 MHz conversation rate, it only consumes 55mW and occupies silicon area of 0.21 mm^2.

DC SPECIFICATIONS

T_j = 25°C, AVDD33 = 3.3 V, DVDD = 1.15V, CLKIN= 320 MHz , unless otherwise noted.

Table 1. DC Performance

Parameter	Test Conditions	Test	Min	Typ	Max	Unit
Resolution		B		12		bits
Monotonicity		B		Guaranteed		
Differential Nonlinearity (DNL)		B		±0.5	±1	LSB
Integral Nonlinearity (INL)		B		±1	±3	LSB
Full-scale Output Current		B		6		mA
Output Common Mode Voltage		B		0.5		V
Output Load Capacitance		B			0.5	pF
Full-scale Output Differential Voltage		B		1.0		Vppd
Gain Matching between IQ channels		B		±0.5		% FS
Offset Error		B			±0.1	% FS
Operating Junction Temperature (Tj)		B(1)	-40		125	°C
Analog Supply High Voltage AVDD33		B	3.0	3.3	3.6	V
Analog Supply Core Voltage AVDD		B	1.09	1.15	1.21	V
Digital Supply Voltage VDD		B	0.99	1.1	1.21	V
AVDD33 Supply Current		B	13	15	18	mA
AVDD Supply Current		B	4	5	7	mA
Power Dissipation		B	44	55	73	mW
Power Down Current		B	10	15	90	uA

(1) Measurement temperature 0~85C

AC SPECIFICATIONS

T_j = 25˚C, AVDD33 = 3.3 V, DVDD = 1.15V, CLKIN= 320 MHz, unless otherwise noted.

Table 2. AC Performance

Parameter	Test conditions	Test	Min	Typ	Max	Unit
Maximum Conversion Rate		B	320			MHz
Signal-to-Noise Ratio (SNR)	f_{out} = 40 MHz	B	64	67		dBFS
Spurious Free Dynamic Range (SFDR)	f_{out} = 40 MHz	B	68	71		dBc
Total Harmonic Distortion (THD)	f_{out} = 40 MHz	B	-67	-69		dBc
Signal-toNoise Distortion (SNDR)	f_{out} = 40 MHz	B	62	65		dBFS
ENOB		B	10	10.5		Bits
Channel Isolation		B	70			dBc
Wake-up Time from Standby mode		B		100		ns
Start-up Time from Power Down (reference is disabled)		B		1		us

Test Categories

A. Preliminary target specification.

B. Simulation of the design over process, voltage, and temperature (PVT)[(1)].

C. Measurements on a set of samples at typical process over voltage and temperature.

D. Measurements on a set of samples at process corners over voltage and temperature.

PIN DESCRIPTION

Table 5. Pin Function Descriptions (total 20 pins)

Index	Pin Name	I/O	Description
1	AVDD33	AP	Analog power supply 3.3V
2	AVDD	AP	Analog power supply 1.15V
3	VDD	DP	Digital power supply 1.1V
4	AVSS	AG	Analog ground for AVDD33 and AVDD
5	VSS	DG	Digital ground for VDD
6	DIN0[11:0], DIN1[11:0]	DI	Digital inputs
7	CLKIN	DI	Clock input
8	IR50U_PN1, IR50U_PN0	AI	50uA reference current input PMOS sent, NMOS received
9	OUTP0/OUTN0	AO	Channel 0 differential outputs (Channel I)
10	OUTP1/OUTN1	AO	Channel 1 differential outputs (Channel Q)
11	PDC[1:0]	DI	DAC channel power down control (logic 1 → power down)
12	PD_STANDBY	DI	DAC standby mode, clock is disabled
13	PD_DAC	DI	DAC power down mode, all blocks are disabled
14	CTRL[15:0]	DI	Programmable control bits
15	CLKO	DO	DAC output clock
16	RESET_DAC	DI	Clock divider RESET signal

P: Power, **G:** Ground, **A**: Analog, **D**: Digital, **I**: input, **O**: Output

OUTPUT LOAD MODEL

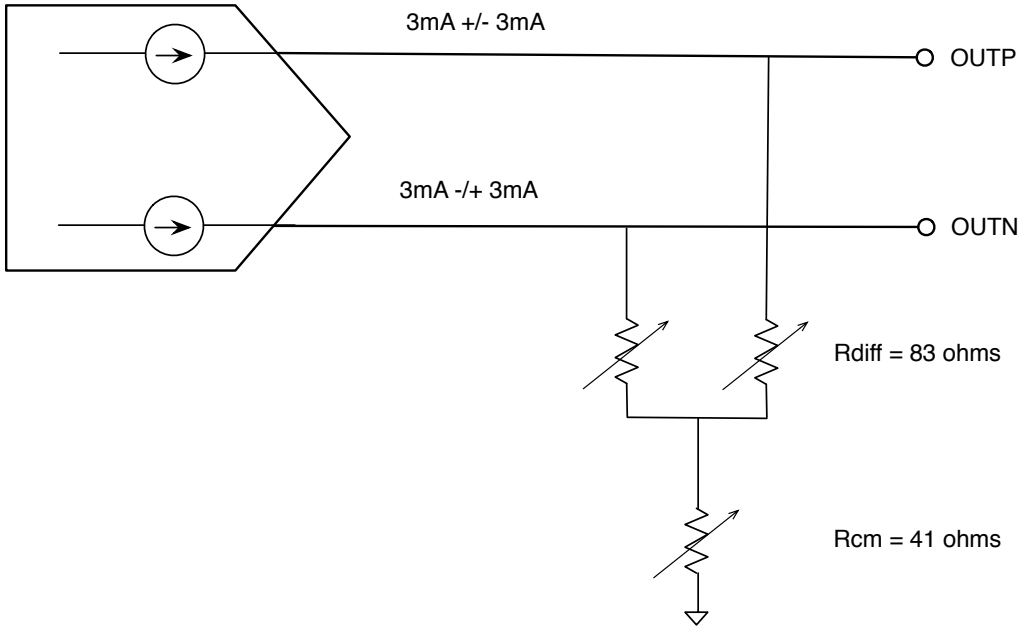

Fig. 2. DAC LOAD MODEL

PHYSICAL DESCRIPTION

IP Macro Layout

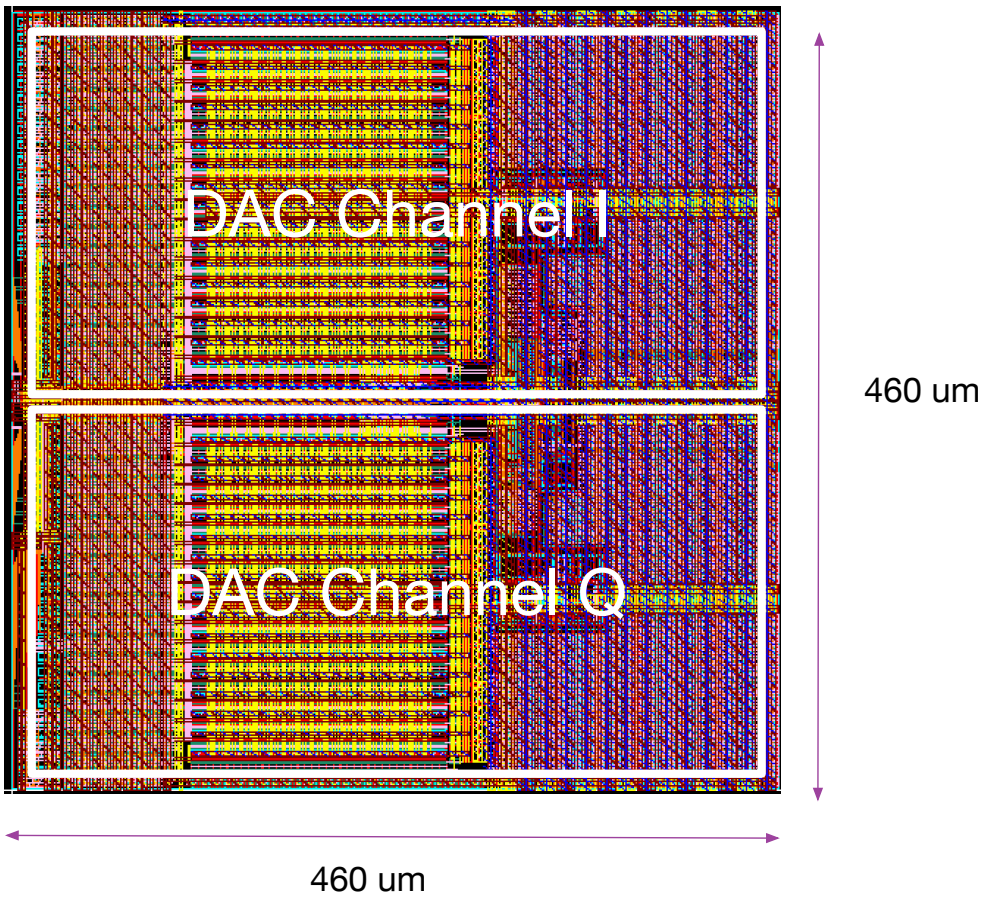

Fig. 3. IP macro layout.