8-Bit 16 MSPS ADC in TSMC350nm

T350_ADC8_16M

FEATURES

- **3.3V Supply Voltage**
- **16 MSPS Conversion Rate**
- **Dynamic Performance @ 16MSPS**
  - **47 dBFS SNR**
  - **-52 dBc THD**
  - **53 dBc SFDR**
  - **ENOB of 7.3**
- **Programmable current setting**
- **Internal Bandgap reference**
- **Ultra Small Core Area: 2.55 mm^2**
- **TSMC 350nm 2P3M**

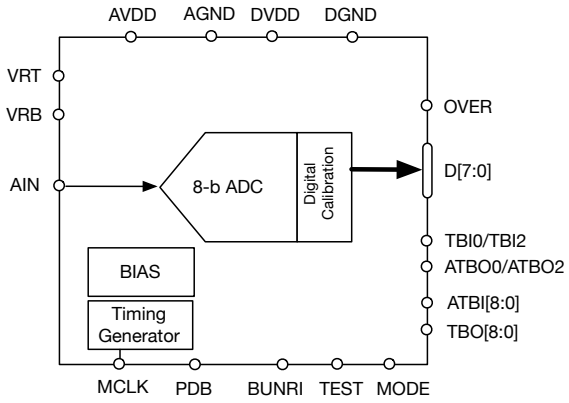


Figure 1. BLOCK DIAGRAM

APPLICATIONS

- **Communication RX Channel**
- **RGB, HDTV, Video Application**
- **Digital Imaging**

GENERAL DESCRIPTION

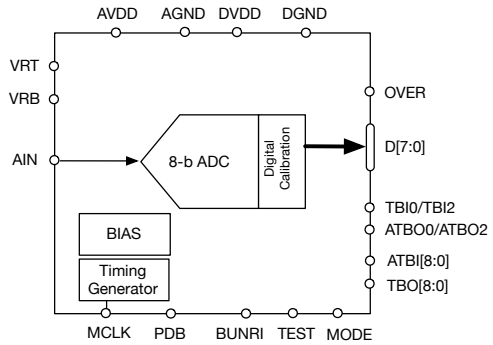
T350_ADC8_16M is compact and low power 8-bit analog-to-digital converter silicon IP. This ADC uses 2.5b/stage pipelined architecture optimized for low power and small area. The ADC is designed for high dynamic performance for input frequencies up to Nyquist rate. This ADC occupies silicon area of 2.55 mm^2. The ADC has high immunity to substrate noise and is ideal for SoC integration.

PIN DESCRIPTION

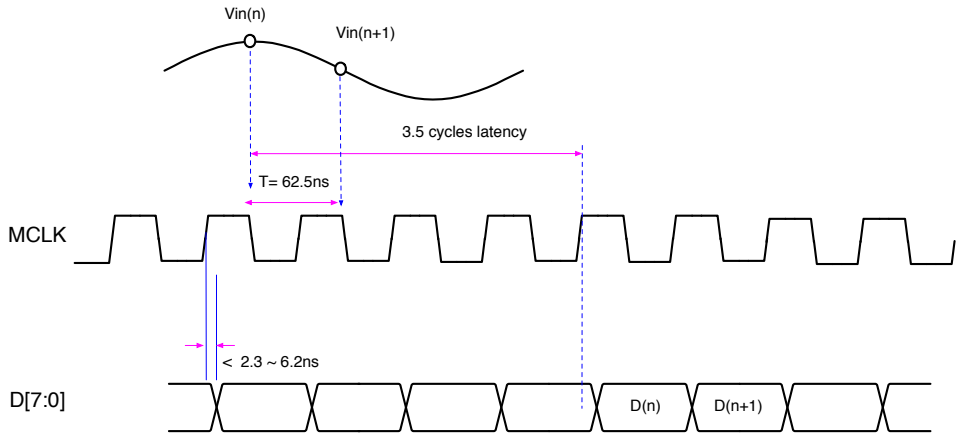
Table 1. Pin Function Descriptions (total 20 pins)

Index	Pin Name	I/O	Description
1	AVDD	AP	Analog power supply 3.3V
2	DVDD	DP	Digital power supply 3.3V
3	AGND	AG	Analog ground
4	DGND	DG	Digital ground
5	VRT	AI	Analog Reference 3.3V
6	VRB	AI	Analog Reference 0V
7	AIN	AI	Analog input (single-end)
8	MCLK	DI	Input clock
9	PDB	DI	ADC powerdown control input (logic 0 → power down, logic 1 → power up)
10	D[7:0]	DO	8-bit output data of ADC
11	OVER	DO	ADC over flow output
12	BUNRI	DI	Test mode selection
13	TEST	DI	Test mode enable, this is used to select ADC test mode
14	MODE	DI	Test mode selection, this is used to select normal operation mode
15	TBI0	DI	Sampling clock input for testing ADC
16	TBI2	DI	Power down input for testing ADC
17	ATBI[8:0]	DI	Overflow and Data input for testing digital block
18	ATBO0	DO	Sampling clock output pin for testing digital block
19	ATBO2	DO	Power down output pin for testing digital block
20	TBO[8:0]	DO	Overflow and Data output for testing ADC

P: Power, **G:** Ground, **A**: Analog, **D**: Digital, **I**: input, **O**: Output



TIMING DIAGRAM



(1) OUTPUT D[7:0] changes at the rising edge of MCLK
(2) The delay of rising MCLK to D[7:0] is 2.3~6.2ns for loading up to 1pF

Figure 2. ADC Timing Diagram

CODE REPRESENTATION

Table 2. Code Description

Analog Input (AIN)	OVER	D[7:0]
< VRB+0.5LSB	0	0000-0000
VRB+0.5LSB to VRB+1.5LSB	0	0000-0001
VRB+1.5LSB to VRB+2.5LSB	0	0000-0010
…	…	
VRB+253.5LSB to VRB+254.5LSB	0	1111-1110
VRB+254.5LSB to VRT	0	1111-1111
VRT<	1	1111-1111

PHYSICAL DESCRIPTION

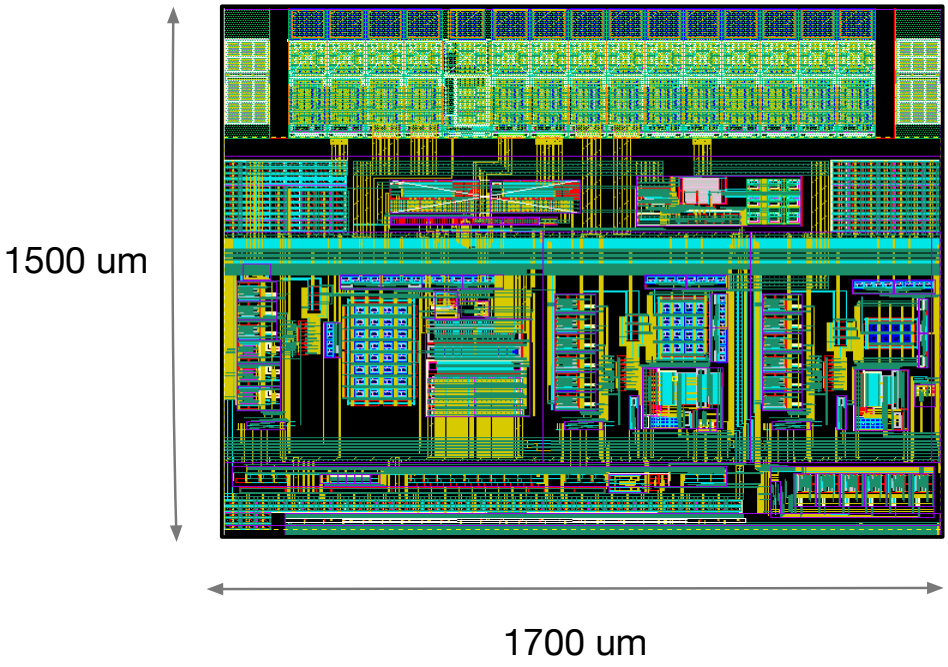


Fig. 3. IP macro layout.

PROCESS

The IP layout (GDSII) is available in the following process and metal stack options.

Table 3. Process Options

Item	Description
Process	TSMC 350nm
Metal Stack	2P3M
Capacitor	PIP cap
Resistor	rpod, rpo2, rnwod
Deep Nwell	No
IO PAD	-

DELIVERABLES

A complete design kit is provided for fast and reliable integration of the IP into customer's design flow. The design kit includes the following:

- Full datasheet
- Physical design database (GDSII format)
- LVS netlist (SPICE compatible)
- Footprint (.LEF format)
- Behavioral model (Verilog model)
- Timing model (.LIB format)
- Integration guidelines and support