IPSmart

12-Bit 160 MSPS Duel ADC in TSMC40LP

IPS_T40_ADC12X2_160M

FEATURES

- **Single Supply 1.15V**
- **160 MSPS Conversion Rate**
- **Current Consumption**
  105 mW @ 160 MSPS
- **Dynamic Performance @ 160MSPS**
  65 dBFS SNR
  -68 dBc THD
  70 dBc SFDR
  ENOB of 10.2
- **Programmable current setting**
- **Programmable full scale**
- **Ultra Small Core Area: 600um X 550 um= 0.33 mm^2**
- **TSMC 40LP 1P7M**

APPLICATIONS

- **WiFi, HDTV, Video Application**
- **Communication RX Channel**
- **Digital Imaging**

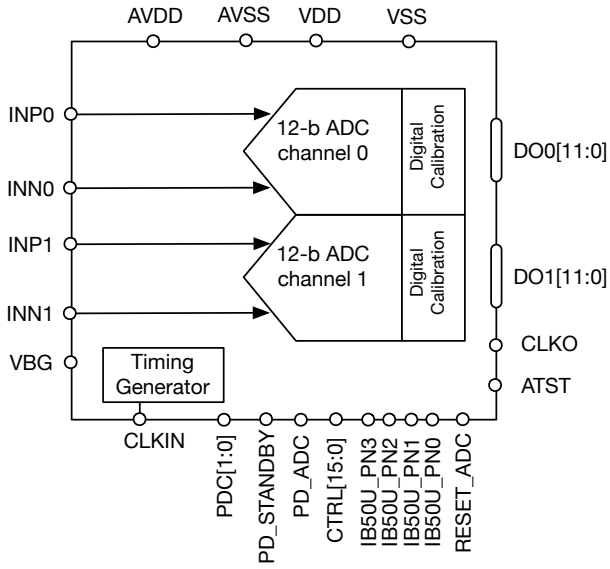


Figure 1. BLOCK DIAGRAM

GENERAL DESCRIPTION

IPS_T40LP_ADC12X2_160M is compact and low power 12-bit analog-to-digital converter silicon IP. This ADC uses 1.5b/stage pipelined architecture optimized for low power and small area. This ADC uses fully differential pipelined architecture optimized for low power and small area. The ADC is designed for high dynamic performance. This ADC consumes 105 mW at 160 MSPS operation and occupies silicon area of 0.33 mm^2. The ADC has high immunity to substrate noise and is ideal for integration into SoC.

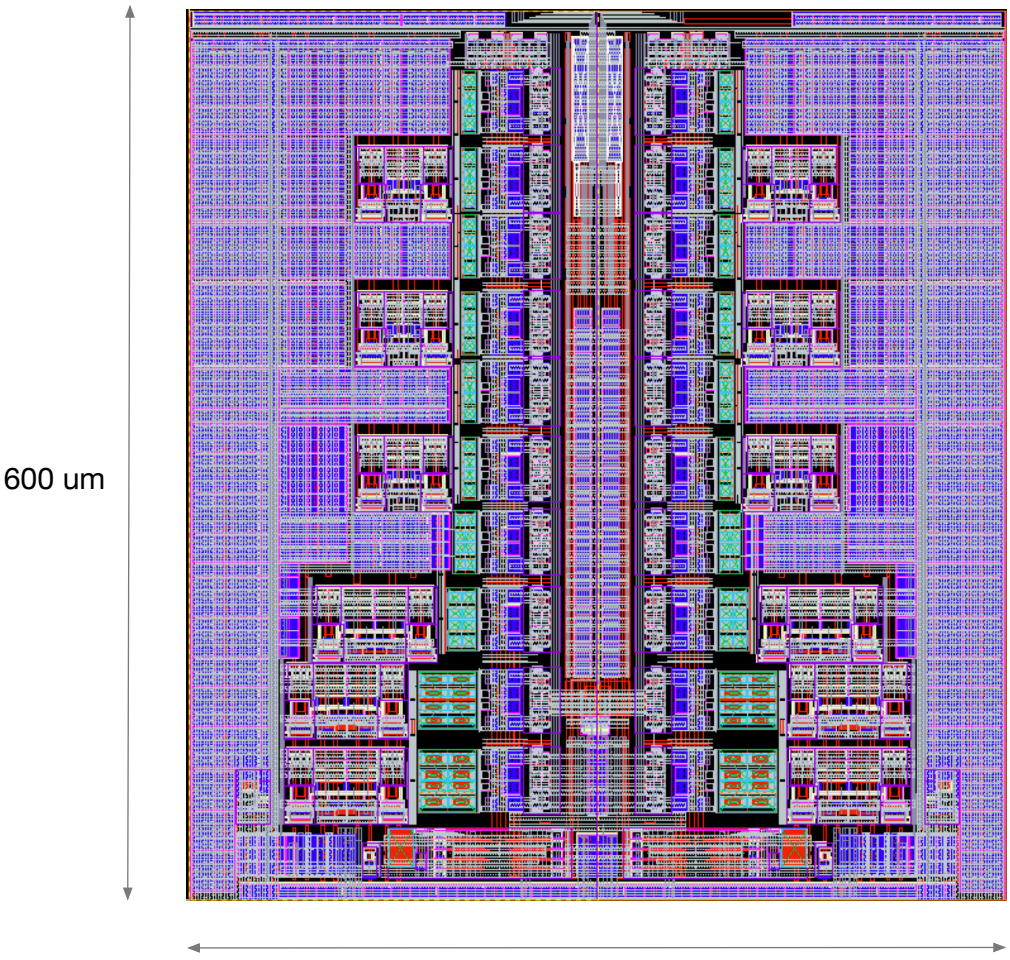
PIN DESCRIPTION

Pin Function Descriptions (total 23 pins)

Index	Pin Name	I/O	Description
1	AVDD	AP	Analog power supply 1.15V from LDO
2	VDD	DP	Digital power supply 1.1V
3	AVSS	AG	Analog ground
4	VSS	DG	Digital ground
5	INP0/INN0, INP1/INN1	AI	IQ Analog differential inputs
6	CLKIN	DI	Input clock
7	PDC[1:0]	DI	ADC channel enable control input (logic 1 → power down)
8	PD_STANDBY	DI	ADC standby mode, clock and OPAMP are disabled
9	PD_ADC	DI	ADC power down mode, all blocks are disabled
10	CLKO	DO	Output clock, can be used to sample DATA[11:0]
11	DO0[11:0], DO1[11:0]	DO	IQ 12-bit output data of ADC
12	ATST	AO	Analog test point
13	VBG	AI	Bandgap voltage input
14	IB50U_PN3, IB50U_PN2, IB50U_PN1, IB50U_PN0	AI	50UA current reference from Bandgap (PMOS → NMOS)
15	RESET_ADC	DI	Clock divider RESET signal
16	CTRL[15:0]	DI	ADC programmability and control bits

P: Power, **G:** Ground, **A**: Analog, **D**: Digital, **I**: input, **O**: Output

PHYSICAL DESCRIPTION



IP macro layout.