IPSmart

12-Bit 320MSPS IQ DAC in TSMC 40nm LP

IPS_T40_DAC12X2_320M

FEATURES

- **Dual 12-bit DAC, up to 320 MSPS**
- **Dual 3.3 V / 1.15 V Supply**
- **Low Power Consumption**
  60mW @ 160 MSPS
- **Superior Dynamic Range**
  71dBc SFDR @ f_{out} = 40 MHz
- **IFS = 6mA with programmability**
- **Output voltage: 1Vppd**
- **Programmable termination resistor**
- **Ultra Small Core Area: 460um X 460um= 0.21 mm^2**
- **TSMC 40LP 1P6M**

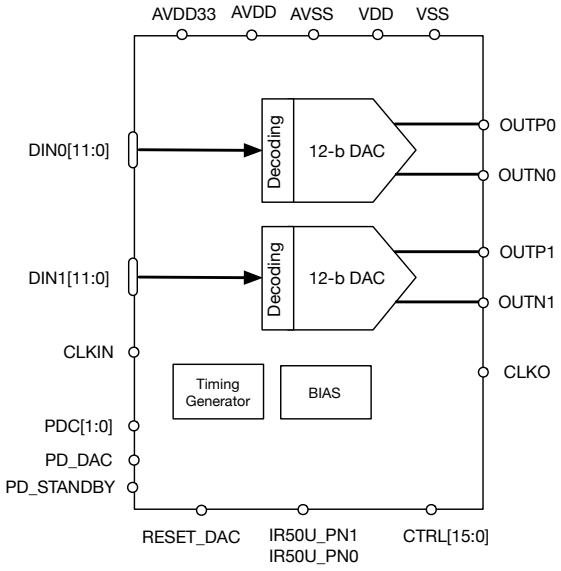


Figure 1. BLOCK DIAGRAM

APPLICATIONS

- **WiFi / LTE / WiMax**
- **Wireless MIMO**
- **Digital Video**
- **Communication Transmit**

GENERAL DESCRIPTION

IPS_T40LP_DAC12X2_320M is compact and low power 12-bit digital-to-analog converter silicon IP in TSMC 40nm LP process. It features two channel current steering DAC.

This IQ DAC IP is optimized for low power and small area. At 320 MHz conversation rate, it only consumes 60mW and occupies silicon area of 0.21 mm^2.

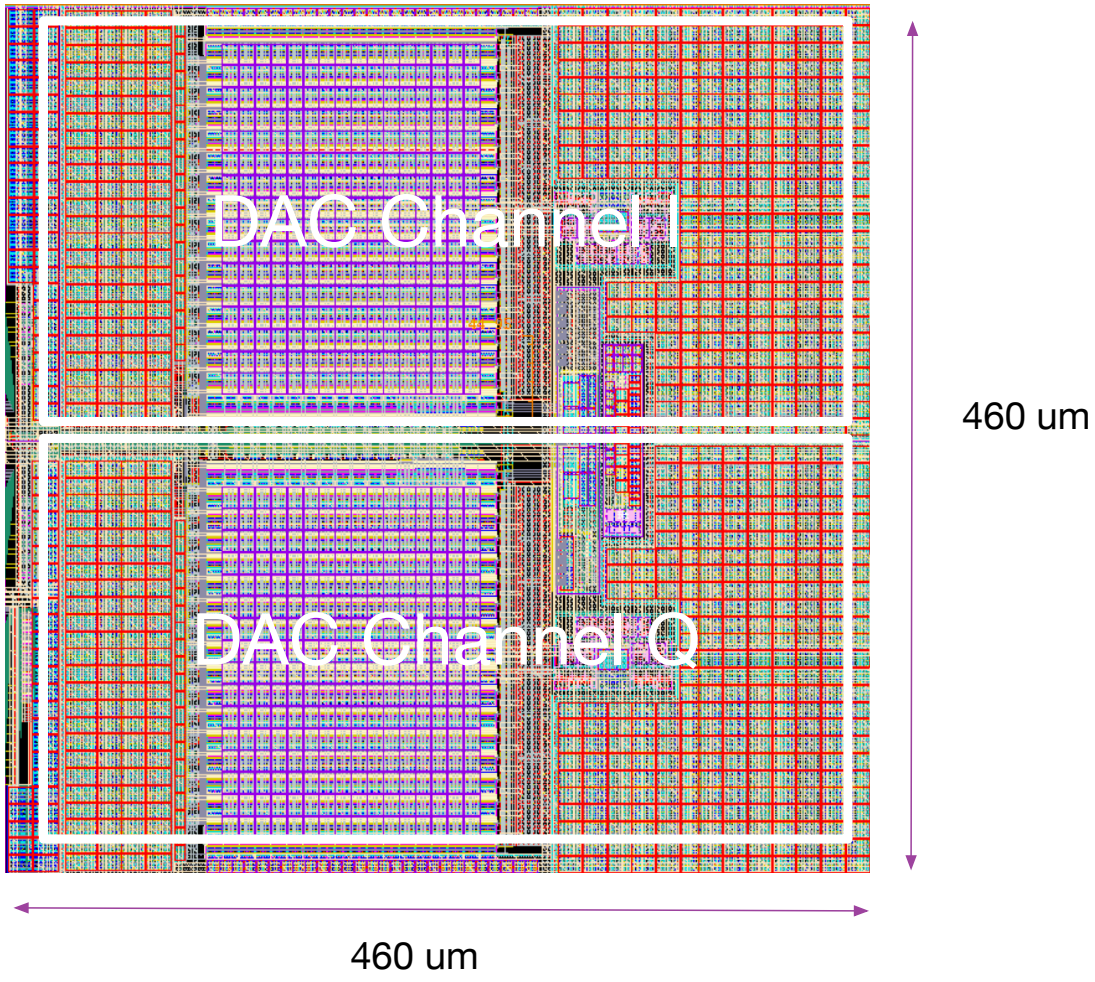
PIN DESCRIPTION

Pin Function Descriptions (total 20 pins)

Index	Pin Name	I/O	Description
1	AVDD33	AP	Analog power supply 3.3V
2	AVDD	AP	Analog power supply 1.15V
3	VDD	DP	Digital power supply 1.1V
4	AVSS	AG	Analog ground for AVDD33 and AVDD
5	VSS	DG	Digital ground for VDD
6	DIN0[11:0], DIN1[11:0]	DI	Digital inputs
7	CLKIN	DI	Clock input
8	IR50U_PN1, IR50U_PN0	AI	50uA reference current input PMOS sent, NMOS received
9	OUTP0/OUTN0	AO	Channel 0 differential outputs (Channel I)
10	OUTP1/OUTN1	AO	Channel 1 differential outputs (Channel Q)
11	PDC[1:0]	DI	DAC channel power down control (logic 1 → power down)
12	PD_STANDBY	DI	DAC standby mode, clock is disabled
13	PD_DAC	DI	DAC power down mode, all blocks are disabled
14	CTRL[15:0]	DI	Programmable control bits
15	CLKO	DO	DAC output clock
16	RESET_DAC	DI	Clock divider RESET signal

P: Power, **G:** Ground, **A**: Analog, **D**: Digital, **I**: input, **O**: Output

PHYSICAL DESCRIPTION



IP macro layout.