IPSmart

12-Bit 125 MSPS Duel ADC in SMIC40L

IPS_S40L_ADC12X2_125M

FEATURES

- **Single Supply 1.15V**
- **125 MSPS Conversion Rate**
- **Current Consumption**
  45 mW @ 125 MSPS
- **Dynamic Performance @ 125MSPS**
  65 dBFS SNR
  -68 dBc THD
  70 dBc SFDR
  ENOB of 10.2
- **Programmable current setting**
- **Programmable full scale**
- **Ultra Small Core Area: 600um X 550 um= 0.33 mm^2**
- **SMIC 40LP 1P6M**

APPLICATIONS

- **WiFi, HDTV, Video Application**
- **Communication RX Channel**
- **Digital Imaging**

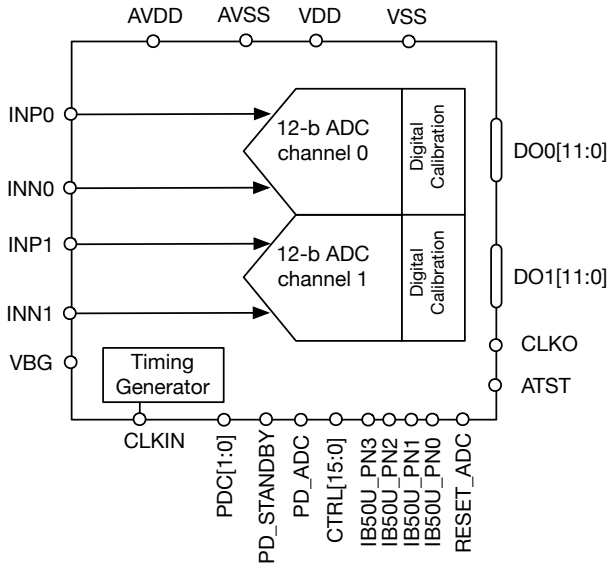

Figure 1. BLOCK DIAGRAM

GENERAL DESCRIPTION

S40L_ADC12X2_125M is compact and low power 12-bit analog-to-digital converter silicon IP. This ADC uses 1.5b/stage pipelined architecture optimized for low power and small area. This ADC uses fully differential pipelined architecture optimized for low power and small area. The ADC is designed for high dynamic performance. This ADC consumes 45 mW at 125 MSPS operation and occupies silicon area of 0.33 mm^2. The ADC has high immunity to substrate noise and is ideal for integration into SoC.

TABLE OF CONTENTS

REVISION HISTORY

Revision	Date	Description
1.0	12/21/2017	Initial revision

DC SPECIFICATIONS

T_j = 25˚C, AVDD = 1.15 V, f_{IN} = 10 MHz, f_S= 125 MHz, A_{IN} = -1 dBFS, unless otherwise noted.

Table 1. DC Performance

Parameter	Test Conditions	Test	Min	Typ	Max	Unit
Resolution		B		12		bits
Monotonicity		B		Guaranteed		
Differential Nonlinearity (DNL)		B		±0.6	±1	LSB
Integral Nonlinearity (INL)		B		±2	±3	LSB
Input Common-Mode Voltage		B	0.45	0.55		V
Input Differential Voltage Range		B		0.9		Vpp
Input Capacitance	single-ended	B		2		pF
Absolute Gain Accuracy		B		±0.5		% FS
Phase mismatch		B		0.5		Degree
Offset Error		B		±4		LSB
Operating Junction Temperature (Tj)		A(1)	-40		125	˚C
Analog Supply Voltage AVDD		B	1.09	1.15	1.21	V
AVDD Supply Current		B	36	39	46	mA
Digital Supply Voltage VDD		B	0.99	1.1	1.21	V
Power Dissipation		B	39	45	56	mW
Power Down Current		B	12	15	40	uA

(1) Measurement temperature 0~85C

AC SPECIFICATIONS

T_j = 25˚C, AVDD = 1.15 V, f_{IN} = 10 MHz, f_S= 125 MHz, A_{IN} = -1 dBFS, unless otherwise noted.

Table 2. AC Performance

Parameter	Test conditions	Test	Min	Typ	Max	Unit
Maximum Conversion Rate		B	125			MHz
Analog Input Bandwidth		B		200		MHz
Signal-to-Noise Ratio (SNR)		B	62	65		dBFS
Spurious Free Dynamic Range (SFDR)		B	68	70		dBc
Total Harmonic Distortion (THD)		B	-64	-68		dBc
Signal-toNoise Distortion (SNDR)		B	60	63		dBFS
ENOB		B	9.5	10.2		Bits
Channel Isolation		B	70			dBc
Wake-up Time from Standby mode		B		100		ns
Start-up Time from Power Down mode		B		1		us

Test Categories

A. Preliminary target specification.

B. Simulation of the design over process, voltage, and temperature (PVT)[(1)].

C. Measurements on a set of samples at typical process over voltage and temperature.

D. Measurements on a set of samples at process corners over voltage and temperature.

DIGITAL SPECIFICATIONS

Table 3. Switching Specifications

Parameter	Test Conditions	Test	Min	Typ	Max	Unit
Clock Duty Cycles		A	48		52	%
Aperture Delay		A		0.2		ns
Aperture Jitter		A		<3		ps rms

CODE REPRESENTATION

Table 4. Code Description for 2's complement

Analog Input (INP-INN)	Hex	Decimal	DATA[11:0] 2's Complement
REFP	7FF	+2047	0111-1111-1111
0	000	0	0000-0000-0000
-REFP	800	-2048	1000-0000-0000

OPERATION MODES

Table 5. Mode of Operation

Mode	Description	Control bits	Recover to normal operation time
Normal operation	All blocks are enabled	PD_STANDBY= PD_DAC= low	N/A
Standby	Clock, OPAMP, BIAS are disabled BG, REF are enabled	PD_STANDBY= high	100 ns (wake-up time)
Power Down	All blocks are disabled	PD_DAC= high	1 us (power-up time)

PIN DESCRIPTION

Table 6. Pin Function Descriptions (total 24 pins)

Index	Pin Name	I/O	Description
1	AVDD	AP	Analog power supply 1.15V from LDO
2	VDD	DP	Digital power supply 1.1V
3	AVSS	AG	Analog ground
4	VSS	DG	Digital ground
5	I_INP/I_INN	AI	I channel differential inputs
6	Q_INP[7:0]/ Q_INN[7:0]	AI	Q channel differential inputs
7	QINPUT_SEL[2:0]	DI	Q channel input selection bits
6	CLKIN	DI	Input clock
7	PDC[1:0]	DI	ADC channel enable control input (logic 1 → power down)
8	PD_STANDBY	DI	ADC standby mode, clock and OPAMP are disabled
9	PD_ADC	DI	ADC power down mode, all blocks are disabled
10	CLKO	DO	Output clock, can be used to sample DATA[11:0]
11	DO0[11:0], DO1[11:0]	DO	IQ 12-bit output data of ADC
12	ATST	AO	Analog test point
13	VBG	AI	Bandgap voltage input
14	IB50U_PN3, IB50U_PN2, IB50U_PN1, IB50U_PN0	AI	50UA current reference from Bandgap (PMOS → NMOS)
15	RESET_ADC	DI	Clock divider RESET signal
16	CTRL[15:0]	DI	ADC programmability and control bits

P: Power, **G:** Ground, **A**: Analog, **D**: Digital, **I**: input, **O**: Output

TIMING DIAGRAM

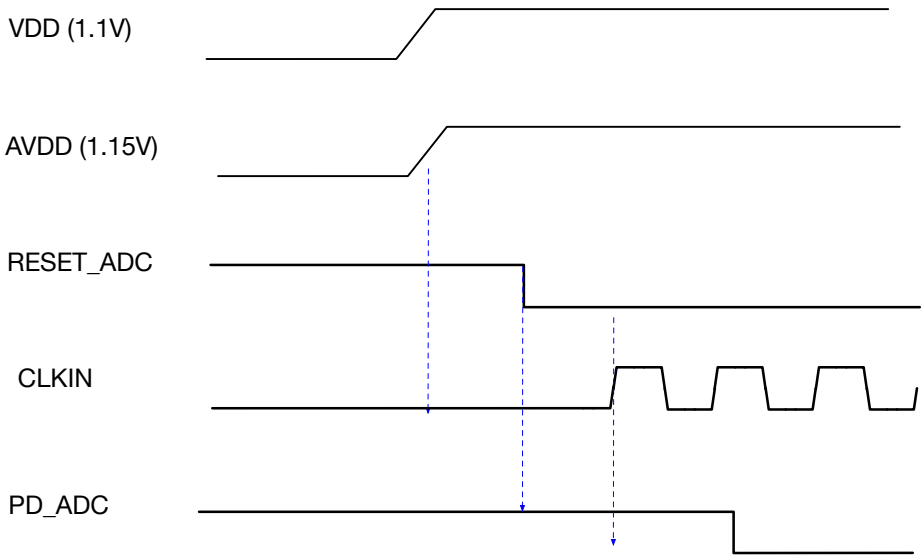

Fig. 2. ADC Power up Sequence

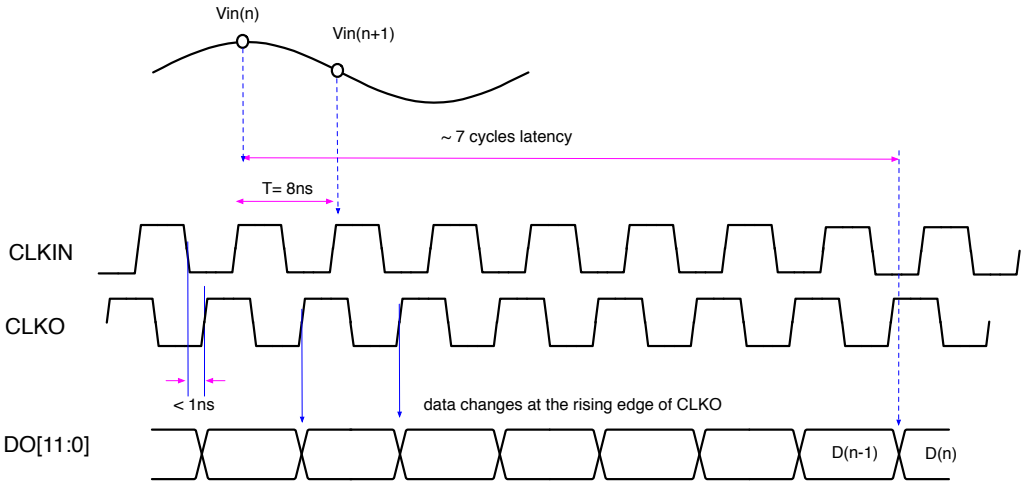

Fig. 3. ADC Timing and pipelined latency

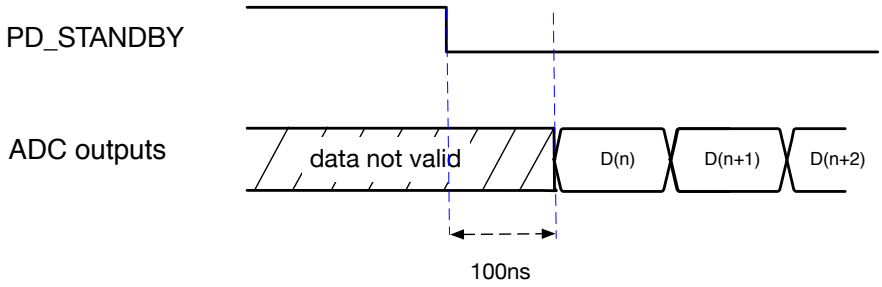

Fig. 4. Timing Diagram of Wake-Up from standby mode

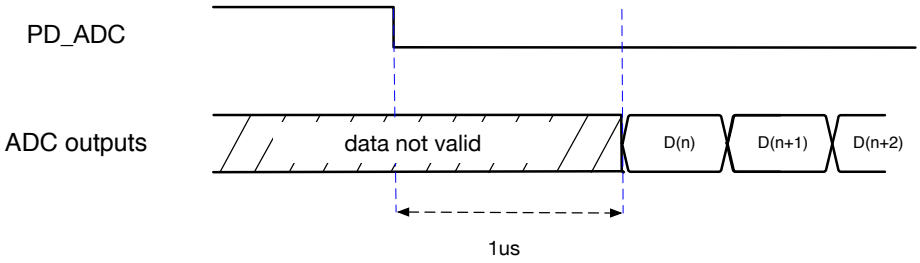

Fig. 5. Timing Diagram of Power-Up from power down mode

CONTROL BITS DESCRIPTION

Table 7. Bias Current Control

CTRL[1:0]	Description	Remarks
11	BIAS Current + 10%	
10	BIAS Current	default
01	BIAS Current -10%	
00	BIAS Current - 20%	

Table 8. OPAMP Bias Current Control

CTRL[3:2]	Description	Remarks
11	OPAMP BIAS + 17%	
10	OPAMP BIAS	default
01	OPAMP BIAS - 17%	For lower sampling rate
00	OPAMP BIAS - 34%	For lower sampling rate

Table 9. ADC Full Scale Control

CTRL[5:4]	Description	Remarks
11	0.95 V	
10	0.90 V	default
01	0.85 V	
00	0.80 V	

Table 10. ADC Internal VCM Control

CTRL[7:6]	Description
1 1	0.58 V
1 0 (default)	0.55 V
0 1	0.52 V
0 0	Not Used

Table 11. ATST Monitor Control

CTRL[9:8]	Description
1 1	VREFP (0.78V)
1 0	VCM (0.55V)
0 1	VREFN (0.33V)
0 0 (default)	Disabled

Note: ATST of two channel ADCs are tied together.

Set PDC[0]=1 to observe ATST voltage on ADC1

Set PDC[1]=1 to observe ATST voltage on ADC0

Table 12. ADC Conversion Rate Control

CTRL[11:10]	Description
1 1	Not Used
1 0	31.25 MSPS
0 1	62.5 MSPS
0 0 (default)	125 MSPS

Table 12. Reserved Control Bit

CTRL[15:12]	Reserved

PHYSICAL DESCRIPTION

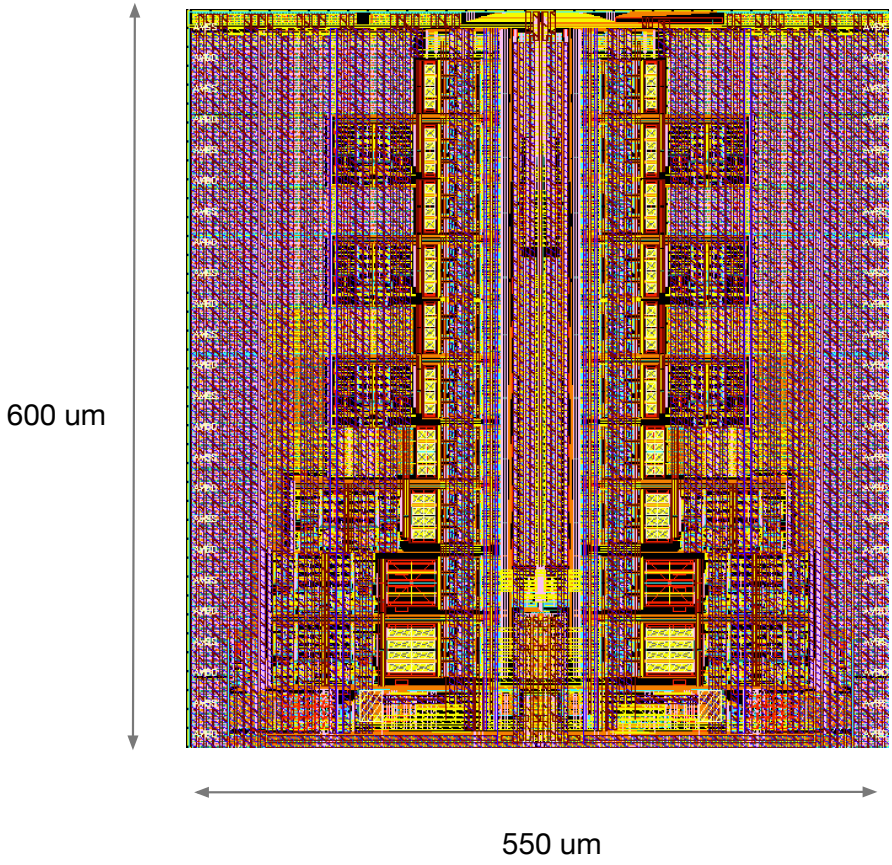

Fig. 6. IP macro layout.

PROCESS

The IP layout (GDSII) is available in the following process and metal stack options.

Table 13. Process Options

Item	Description
Process	SMIC 40nm LP
Metal Stack	1P5X1U
Capacitor	MOMCAP
Resistor	RPPOLY
Deep Nwell	No
IO PAD	-

DELIVERABLES

Complete design kit for fast and reliable integration of the IP is provided. The design kit includes the following:

- Full datasheet
- Physical design database (GDSII format)
- LVS netlist (SPICE compatible)
- Footprint (.LEF format)
- Behavioral model (System Verilog model)
- Timing model (.LIB format)
- Integration guidelines and support